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Modeling of Electroceramics—Applications and Prospects

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Abstract

Modeling of electronic materials and devices takes place on three different levels: (1) the device functions which are linked to the electronic circuit, (2) the solid state physics which relates the microscopic and macroscopic properties, and (3) the processing which is employed to build up the material and the device. On all three levels, Si-based semiconductor technology today extensively relies on comprehensive models implemented in detailed simulation tools. Due to the much higher complexity in composition and structure, as well as the huge spectrum of functions, the modeling of electroceramic materials and devices is still in its infancy. Currently, we see a trend towards enhancing electroceramics modeling efforts mainly to support the numerous activities of integrating this class of materials into the Si world. This review covers selected examples of integrated electroceramic thin film devices which demonstrate the present state-of-the-art. Emphasis is placed on the understanding of the statics and dynamics of the ferroelectric polarization as well as on properties originating in the defect structure of the perovskite lattice. The review attempts to identify fields where great improvements have been made in recent years, 'blank' areas of lack of understanding, and trails which might be employed to anticipate future developments. © *1999 Elsevier Science Limited. All rights reserved*

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1 Introduction

Among functional materials, such as semiconductors, metals, polymers, and glasses, electronic ceramics are probably the class of materials with the widest variety of functionalities. Even if only the major material properties are taken into account, the spectrum comprises ferroelectric properties for application in non-volatile memories and FE field-effect transistors (FET), piezoelectric properties for microsensors, microactuators, micromotors and surface acoustic wave devices, and pyroelectric properties for IR detectors and IR image devices. Furthermore, there are oxides (e.g. TiO_2) with appropriate electronic band structures and surface states rendering them useful for photoelectrochemical solar cells, ionically conducting oxides for gas sensors and solid oxide fuel cell (SOFC) electrolytes, mixed ionically-electronically conducting oxides for semi-permeable gas membranes and SOFC electrodes, semiconducting oxides for temperature sensors and transparent FETs, and metallically conducting oxides for linear resistors and corrosion resistant conductors. In the past decade, HTSCs have attracted huge attention. Today, HTSC thin films are employed for SQUID sensors and for low-loss coatings in microwave resonator systems. Magnetic properties of transition metal oxides, such as $(La,X)MnO_3$, $X = Ca$, Sr, Ba, are investigated for their colossal magnetoresistive effect. Electrochromic properties of oxides are employed for display applications and electro-optical properties are studied for optical waveguides and modulators. Low permittivity materials are required for packages and interlevel dielectrics on chips, while high-permittivity oxides will be used for high-density charge storage applications such as decoupling capacitors or DRAM cell capacitors. For more details on the material's background, the reader is referred to Refs. 1–3 while Refs. 4–7 emphasis device and processing aspects.

The most recently introduced product based on integrated electroceramic thin films is the RF-operated smart card which makes use of a non-volatile ferroelectric random access memory (FeRAM).[8] These smart cards—unlike ordinary

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credit cards—not only store but also process data by an embedded microcontroller. They are anticipated for use in public transportation and traveling, electronic banking and sales, as well as in intelligent production and logistics with an expected high impact on daily life in the coming decade.

Figure 1 shows the functional principle of a smart card in a block diagram. At the approach of a card, a smart card reader provides an RF connection which fulfills two purposes: (1) electrical *energy* is fed into the card since the card itself has no battery and (2) data exchange is performed by modulation on the RF signal.

The RF signal is rectified and the energy is stored in a reasonably sized thin-film capacitor. The voltage control module supplies the dc power to all other modules of the card, i.e. the modulator/demodulator for the RF signals, the microcontroller, some control logic, and the non-volatile memory.

In this review, we consider the possible advantages of the use of electroceramic thin-film components in smart cards. A FeRAM is most suitable for data storage since the memory of the card has to be fast, non-volatile, and compatible with low-voltage operation. For the dc energy storage, a high-k thin film capacitor may be considered because of the required large capacitance value. Both, the high-k storage capacitor and the low density FeRAM array, will be employed throughout this review to explain some relevant aspects of the modeling and simulation required for the integration of electroceramic functions. Figure 2 sketches the three levels of simulation models to be considered.

On the level of the circuit simulation model, the designated electrical circuit is completely tested with respect to its static and dynamic behavior. Every component of the circuit—including every parasitic component—is described by (integral) parameters without any information about the physical realization of the component on the chip.

In fact, the physical and geometrical realization is treated on the second level, the device simulation model. For instance, the FE capacitor on the chip is designed to consist of a given ferroelectric material, to have a certain dielectric thickness and area to obtain the parameters required by the circuit design. In the device simulation model typically finite-element methods (FEM) are employed and the electrical, thermal, mechanical and all coupled properties at each mode of the FEM grid are taken into account.

Finally, the device has to be processed. For the process technology steps involved, such as solution-based or vapor-phase-based deposition, thermal processing, etching etc., the third level of simulation models is required for assistance in chip development.

The model levels are interlinked: On the route down, each level sets the requirements for the next level. On the way up, every simulation model sets the boundary conditions for the previous level. All models may be only empirical, however, the more the models are based on a physical understanding the more powerful they become. This paper will discuss all three levels of modeling with an emphasis on the second level since it is the most relevant level for materials science.

2 Circuit Simulation

In the circuit simulation model, a high-k dielectric such as $(BaSr)TiO_3$ gives rise to an equivalent-circuit presentation, which consists of a field-dependent

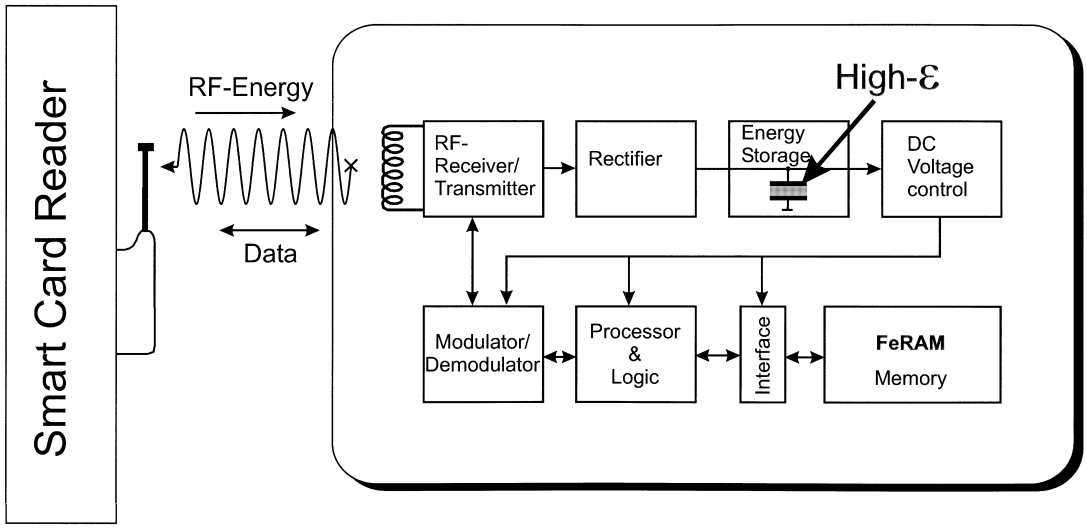

Fig. 1. Functional units of a smart card—potentially with an electroceramic high-permittivity thin film capacitor for temporary energy storage and a ferroelectric non-volatile memory.

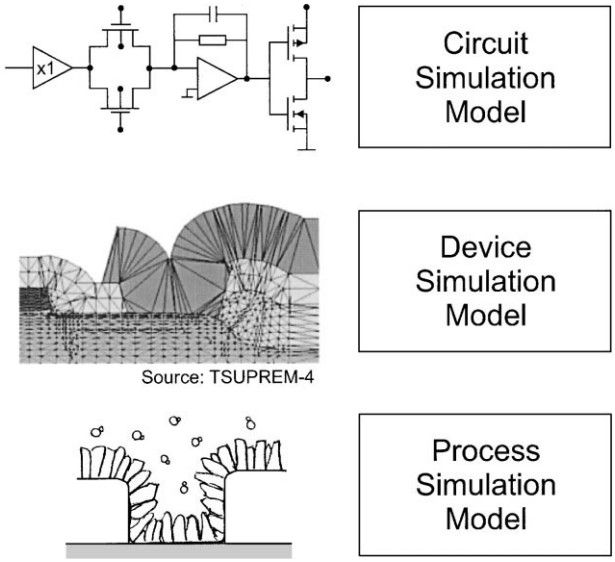

Fig. 2. Illustration of the levels of modeling for technology development in microelectronics.

high-frequency capacitance and an infinite RC line with distributed RC times in which the capacitances are non-linear again. This relaxation impedance gives rise to the Curie–von Schweidler behavior as described in detail in Refs. 9 and 10. In parallel, there is a non-ohmic leakage resistance.[11,12] Temperature and (mechanical) stress dependencies have to be taken into account for all elements.[13,14]

The circuit simulation model will completely resolve the FE memory array (Fig. 3) diagram into all individual components as shown, for example, for one single FeRAM cell. The FE capacitor is not covered by traditional semiconductor circuit simulators. Therefore, a realistic equivalent representation has to be implemented as sketched in Fig. 4. The ideal FE capacitor is supplemented by non-linear, non-hysteretic dielectrics, a relaxation impedance with a hysteretic contribution which may limit the effect of the speed of the reliable separation between logical '0' and '1' states in high-speed FeRAM circuits.[15,16] In addition, a leakage resistance has to be taken into account.

3 Device Simulation

The device simulation model considers the physical and geometrical realization of the device on a chip. Figure 5 shows a FeRAM offset cell as an example. In the cross section, there is the Si CMOS level including all logic components (such as the access transistor, etc.), as well as the level of the interlevel dielectrics (ILD). The ILD level separates the Si level from the topmost level comprising the FE capacitors and the metallization. For the device simulation, a suitable finite-element grid is imposed on the designated structure. This grid will have a variable mesh width being more dense at sites with high gradients or critical electrical, mechanical and thermal conditions. For the purpose of this review, the FE thin film will be considered more closely. The basic ferroelectrical properties of FE thin films are primarily determined by the domain pattern and the resulting domain switching pathways. Figure 6 sketches the orientational possibilities of (tetragonal) PZT films in the initial unpoled and in the poled state. The poling can proceed in principle by 180° domain switching, 180° domain shifting, and 90° domain shifting. In (111)-oriented films, there are no constraints on the poling mechanisms which may lead to a single domain state for epitaxial films. In the (001)/(100) orientation, the initial state depends on the difference of the thermal

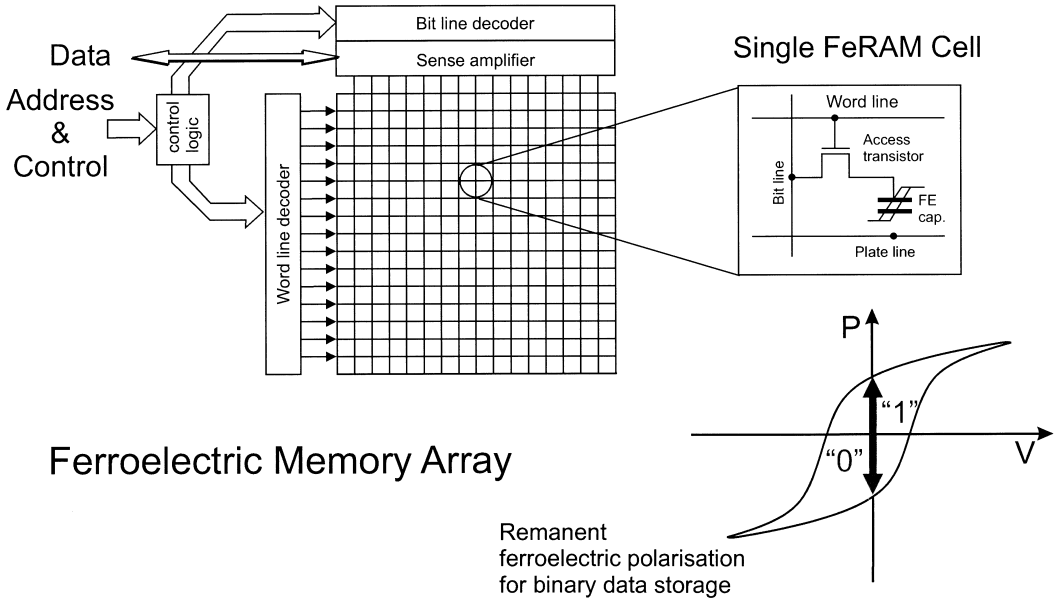

Fig. 3. Operating principle of the non-volatile FE memory array.

expansion coefficients of the film and the substrate. This sets the film under compressive stress, resulting in a predominantly *c*-axis (001) orientation, or under tensile stress, resulting in a predominantly *a*-axis (100) orientation. In both cases, the 90° domain wall shifting is suppressed since this would lead to a ferroelastic deformation of the film in the plane. Obviously, this is hardly possible due to the 2D damping. Details on the substrate influence and growth of oriented PZT films are described by Wouters,[17] Muralt *et al.*,[18] Kingon *et al.*[19] In addition, the basic relations as well as the microscopic implications for the film substrate interface are given by Speck *et al.*[20] The domain-switching mechanisms and the related constraints in thin films also affect the reversible and irreversible contributions of the FE polarization and, hence, the electric small and large signal response behavior, which has to be taken into account in a detailed device model. The large signal P–V behavior (Fig. 7) is recorded by sweeping the voltage excitation over the full range and integrating the current response by means of a Sawyer–Tower or virtual ground circuit using an aixACCT TF analyzer. The

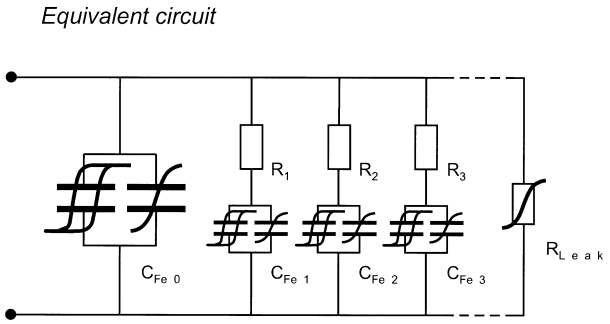

Fig. 4. Detailed equivalent circuit representation of an FE cell capacitor covering the frequency dependence of the *P–V* and the *C–V* characteristics, the Curie–von-Schweidler-type relaxation impedance, and the leakage resistance.

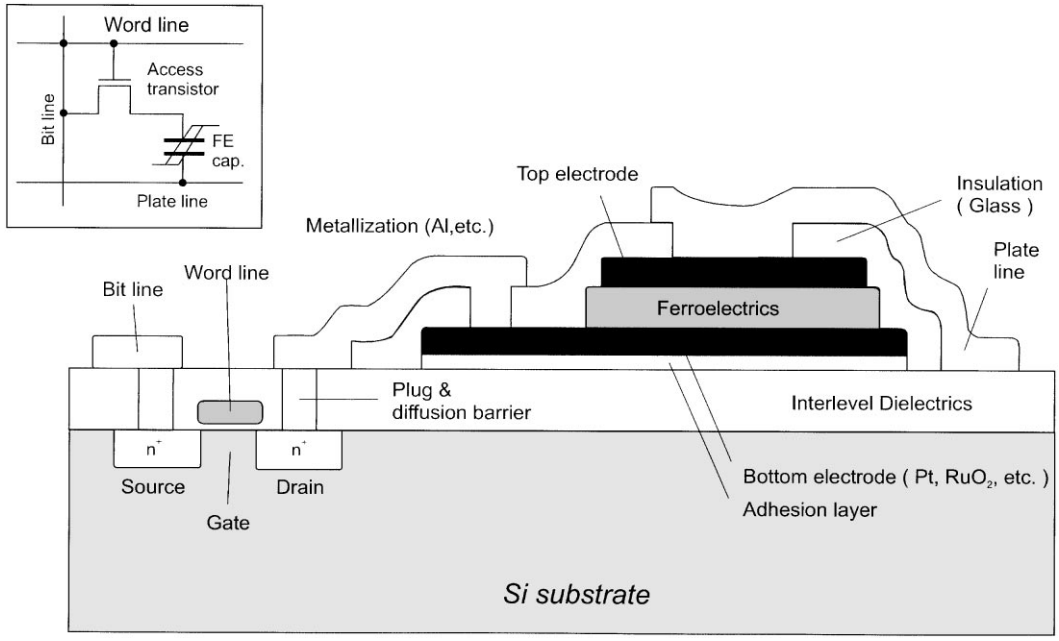

Fig. 5. Cross-sectional sketch of a (low-density) offset FeRAM cell.

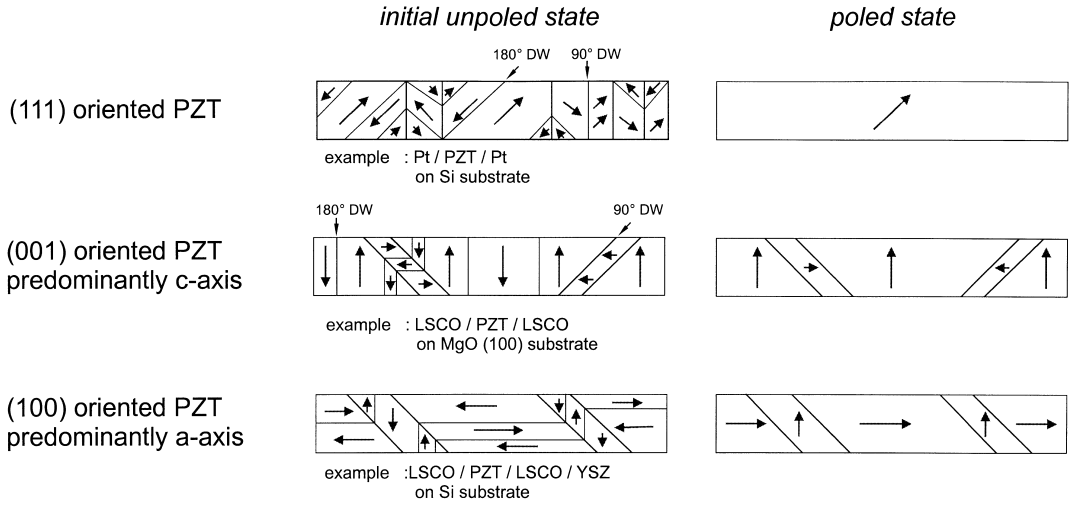

Fig. 6. Possible crystallographic and domain orientations of PZT thin films (see text for refs).

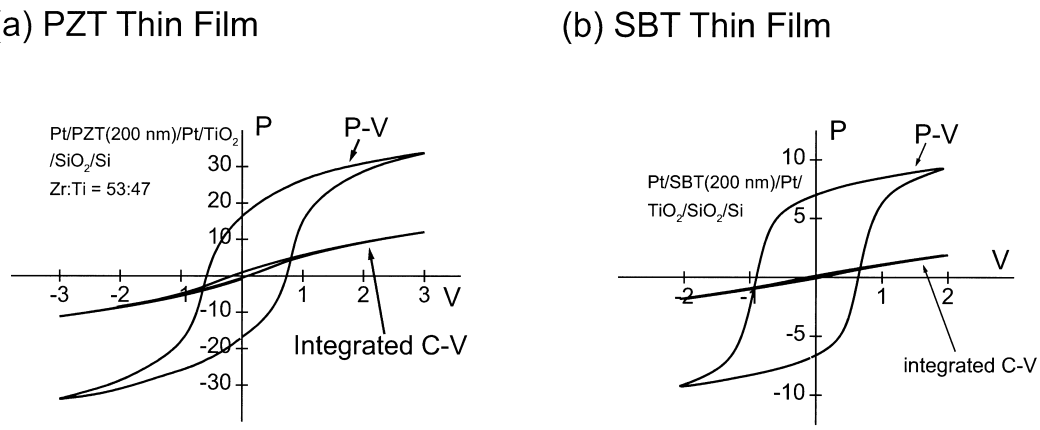

Fig. 7. Separating the reversible and irreversible contributions to the ferroelectric polarization of predominantly (111)-oriented PZT and randomly oriented SBT films by means of P–V and (integrated) C–V measurements.[23]

resulting P–V curve comprises reversible *and* irreversible contributions, P_{rev} and P_{irr}, to the FE polarization. The slope of the P–V curve is given by the dielectric susceptibility

$$\chi_{diff} = \frac{dP}{\varepsilon_o dE} = \chi_{rev} + \chi_{irr}$$

which can be divided into the two contributions. Recording the C–V behavior qualitatively by means of a small ac signal and a dc bias sweep will only trace the reversible contribution, χ_{rev}. An integration leads to

$$P_{rev}(V) = \frac{1}{A}\int C(V)dV$$

where A is the electrode area and P_{rev}–V shows a hysteretic behavior similar to the total P–V curve.[21] To obtain a precise separation between P_{rev} and P_{irr}, the curves have to be recorded as a function of the ac and sweep frequencies and appropriate extrapolations have to be performed.[22] A comparison of the P–V and P_{rev}-V behavior for (a) a predominantly (111)-oriented $Pb(Zr,Ti)O_3$ (short: PZT) film and (b) a polycrystalline, granular $SrBi_2Ta_2O_9$ (short: SBT) film is shown in Fig. 7.[23] The relatively small reversible contribution to the total polarization in the case of the SBT films is possibly due to the fact that this material predominantly shows 180° domains.

In the case of the energy storage capacitor, the microstructure of the $BaTiO_3$ or $(Ba, Sr)TiO_3$ thin film exhibits a strong influence on the permittivity and its temperature dependence. By precisely tuning and controlling the process parameters of the CSD routes it is possible to realize $BaTiO_3$ films in a range from granular, nanocrystalline microstructures to columnar textured microstructures (Fig. 8). Details of the preparation and characterization of these films are described in Refs. 24 and 25.

In Fig. 9, the grain-size dependence of the permittivity at room temperature is compiled from different sources.[26–28] As found for $BaTiO_3$ bulk ceramics, the permittivity exhibits a pronounced maximum at an average grain size of approx. 800 nm. Obviously, this maximum results from the superposition of two effects. Firstly, below the grain size of few μm the average permittivity of the grain interior increases due to a stress effect as shown by Buessem *et al.*[29] Secondly, the drop of ε_r, below approx. 800 nm may be interpreted by an interfacial layer effect at the grain boundaries as proposed recently by Frey and Payne[27] using a dielectric brick wall model. From their data, a low-permittivity layer of 0·8 to 2 nm thickness and ε_{rGB} values in the range from 90 to 130 can be calculated. Compared to the bulk ceramics of Frey and Payne,[27] thin $BaTiO_3$ films of the same average grain size show a significantly lower permittivity. This difference can be explained by a combination of effects. Firstly, the low-permittivity interface effect seems to be more pronounced at the $BaTiO_3$/Pt electrode interface than at grain boundaries in $BaTiO_3$[30]. This electrode interface effect has additionally been revealed by investigations on, for example, the thickness dependence of the C–V behavior[31,32] and studies of the dielectric function at optical wavelengths for films of $SrTiO_3$ as an incipient ferroelectric.[33] Secondly, the $BaTiO_3$ and $(Ba,Sr)TiO_3$ films deposited on platinized Si wafers are under considerable tensile stress. The corresponding electrostrictive effect results in a significant reduction of permittivity as quantitatively shown in Refs. 13 and 14. Finally, any deviation from the stochiometric Ba/Ti ratio leads to a contribution to the ε_r suppression.[13]

For thin films, modeling has to take into account the fact that the phase diagram is influenced by constraints such as the 2D clamping. For epitaxial

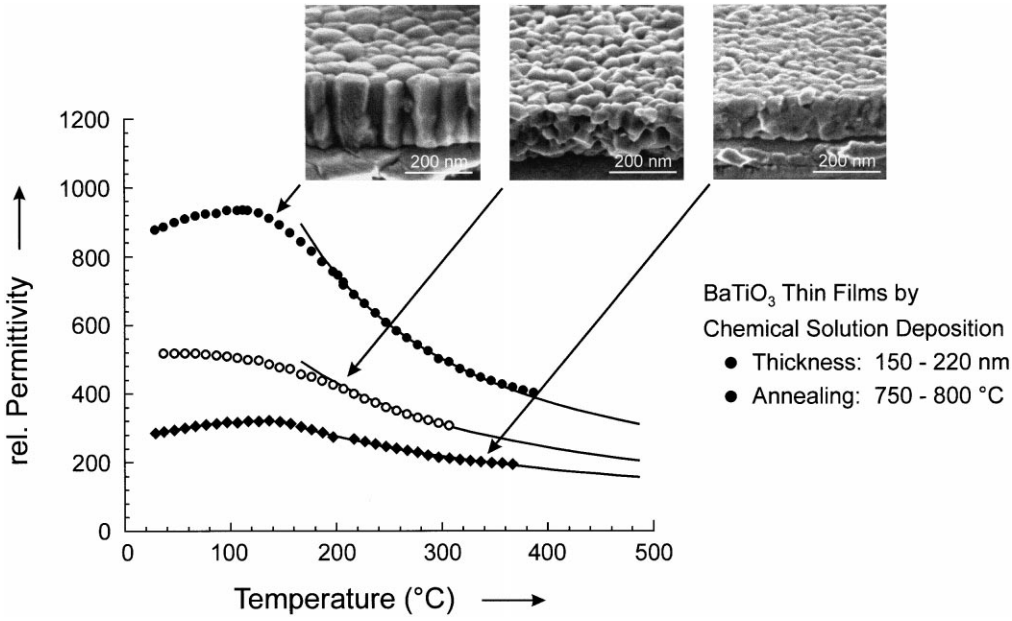

Fig. 8. Temperature dependence of the permittivity for $BaTiO_3$ thin film prepared (from right to left) with nanocrystalline, coarse-grained polycrystalline, and columnar microstructure prepared by CSD.[24,25]

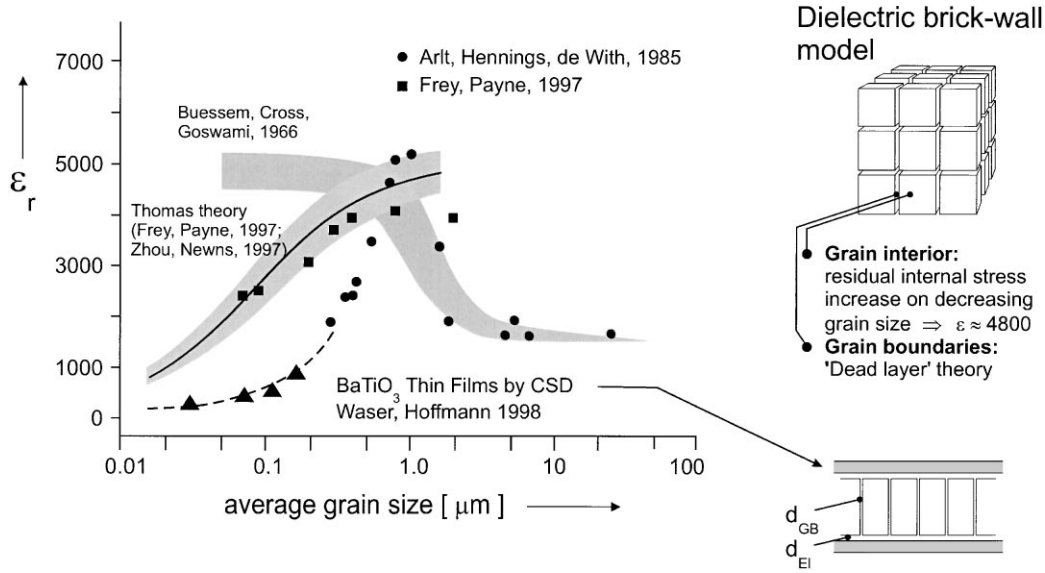

Fig. 9. Grain size dependence of the permittivity of $BaTiO_3$ bulk ceramics (squares, circles) and thin films (triangles) at $T = 289$ K.

$BaTiO_3$ films on cubic substrates, the phase diagram has been calculated by Pertsev *et al.*[34] as a function of the misfit strain (Fig. 10). This model has been successfully modified to describe the ε_r-T behavior of our columnar structured $BaTiO_3$ and $SrTiO_3$ films.[35]

To further increase the capacitance per unit area on a chip, the concept of the traditional monolithic multilayer capacitors (MLC) may be applied to the thin film technology as described in Ref. 36 for a capacitor stack on a MgO substrate. Figure 11 shows an example of thin films in a multilayer structure (TMC) realized by chemical solution deposition of the dielectric layers (e.g. $SrTiO_3$), etching of the contact holes, and metallization on a Si wafer.[37] In the case of large structures, *wet* etching and metallization through shadow masks is sufficient. For small structures, lithography and *dry* etching techniques are required.

Especially if dielectric materials with very high permittivity values are employed, many non-ideal properties have to be considered in the simulation models. Specifically, the electromechanical coupling by the piezoelectric and electrostrictive effect, the electrothermal coupling by ac and dc dissipation effects, and the mechanothermal coupling by differences in the thermal expansion coefficient are to be taken into account. Using conventional X7R-type ceramic multilayer capacitors, an FEM simulation program has been developed which employs all relevant dielectric, thermal, and mechanical properties, and the complete set of coupled properties.[38] As an example, the impedance spectrum is shown in Fig. 12 for a X7R-type capacitor under

dc bias load. In addition to the curve of a slope of −1 which describes an ideal capacitor, there are many electrostrictive resonances. For a TMC, a simulation is required to adjust the geometry in such a way that resonances are avoided at the operating frequency of the device.

For a complete modeling of the electronic properties of electroceramic materials, the defect structure and the correlated influence of the microstructure has to be considered. Based on the disorder of the unperturbed crystal lattice (i.e. the interior of the grains) and on the crystallographic

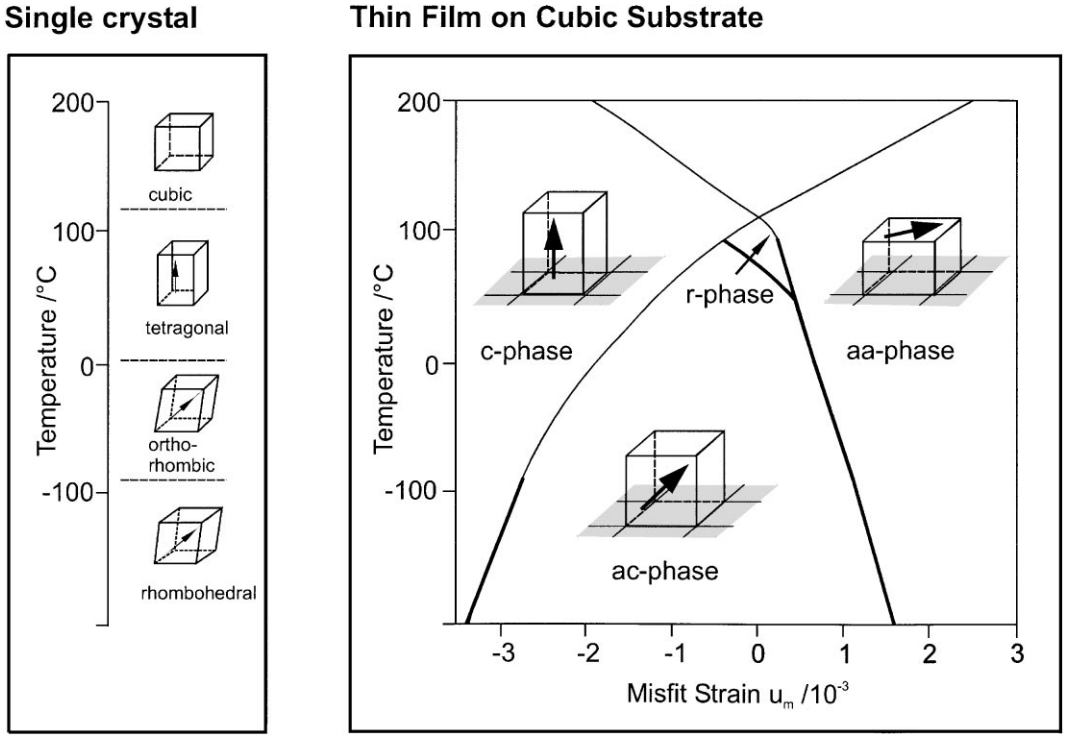

Fig. 10. Phase diagram for $BaTiO_3$: (a) bulk single crystal and (b) epitaxial thin films grown on cubic substrates of high temperatures (redrawn from Ref. 34 and illustrated).

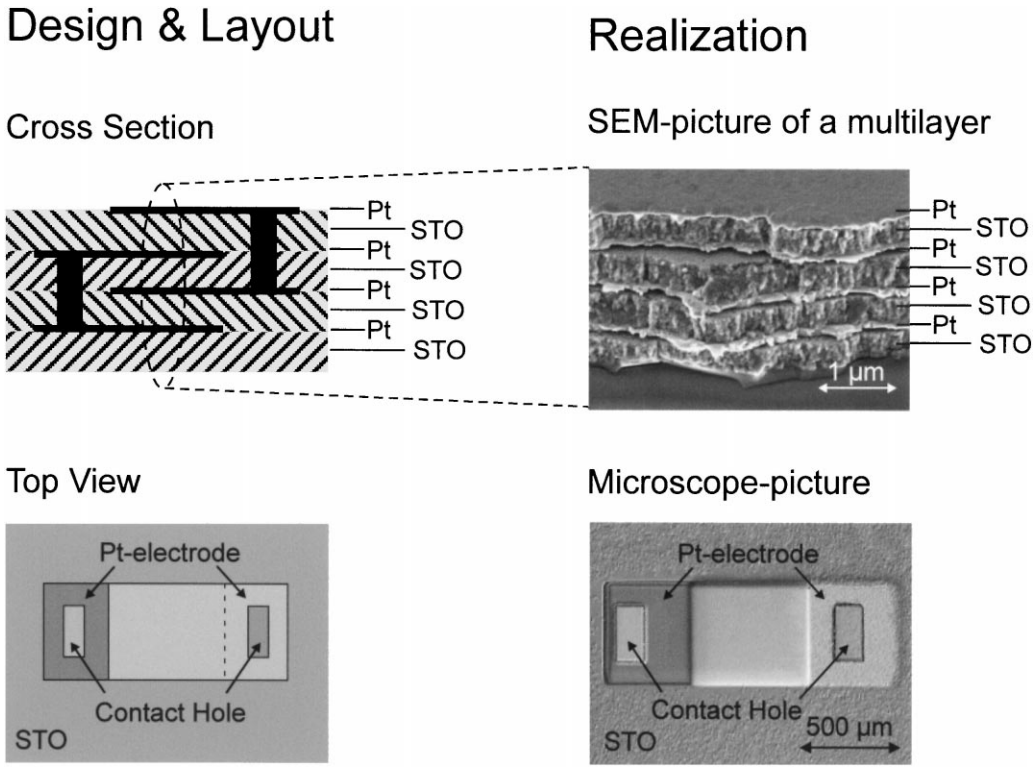

Fig. 11. Design, layout, and realization of a thin film multilayer capacitor concept using sputtered Pt electrodes and CSD-synthesized $SrTiO_3$ dielectric layers.[37]

structure of the grain boundary region [Fig. 13(a)] as well as the segregation of dopants during sintering, the formation of space charge layers, the electronic and ionic charge transport *across* grain boundaries, the formation of inversion regions, and the transport *along* grain boundaries are to be calculated. In Fig. 13(b), an example of a simulation study of acceptor-doped $SrTiO_3$ is shown. Using the set of mass action equations of all relevant defect equilibria as well as the Fermi–Dirac statistics and the Poisson equation, the concentration and valency states of the defects are calculated. This is used to determine the band bending and the local conductivities and can be employed to explain all details of the temperature dependence of the admittance spectra and the grain boundary resistance as described in Ref. 39. In thin films, the point defect structure is different to the bulk systems due to the significantly lower processing temperatures. In addition, specific twin boundaries and dislocations have to be taken into account.[40] In summary, a comprehensive device simulation based on the physical understanding of the materials has to span a bridge between the macroscopic scale of the complete device and the microscopic scale of the atomic structure.

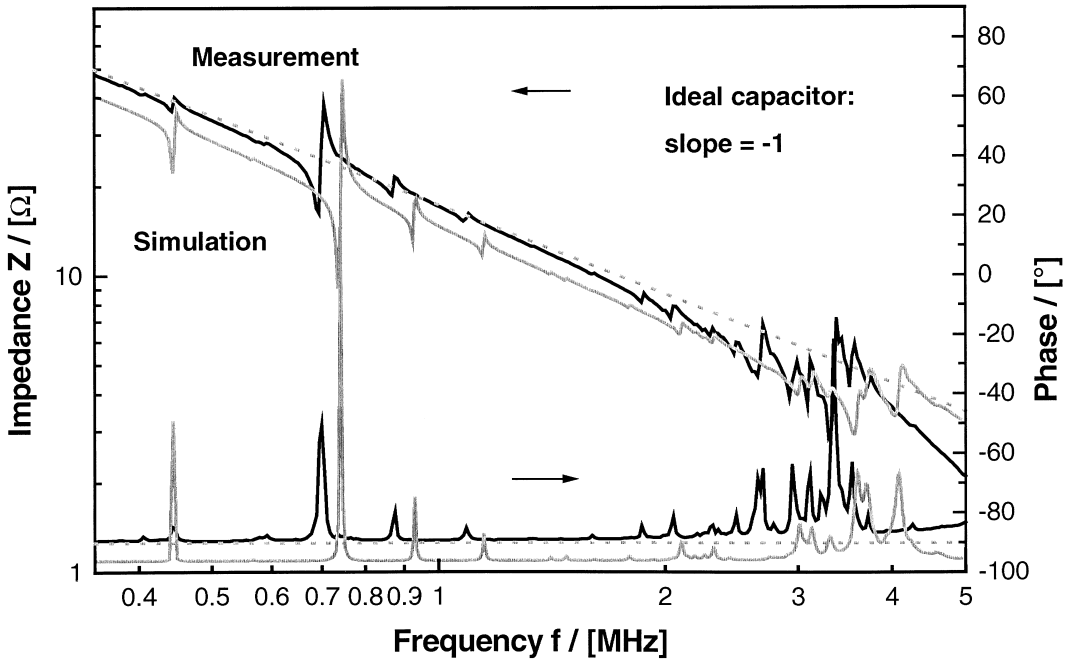

Fig. 12. Impedance and phase spectra for an X7R-type ceramic multilayer capacitor under dc bias consisting of the curve for an ideal capacitor, as well as the measured and simulated behavior showing a large variety of geometrical resonances.[38]

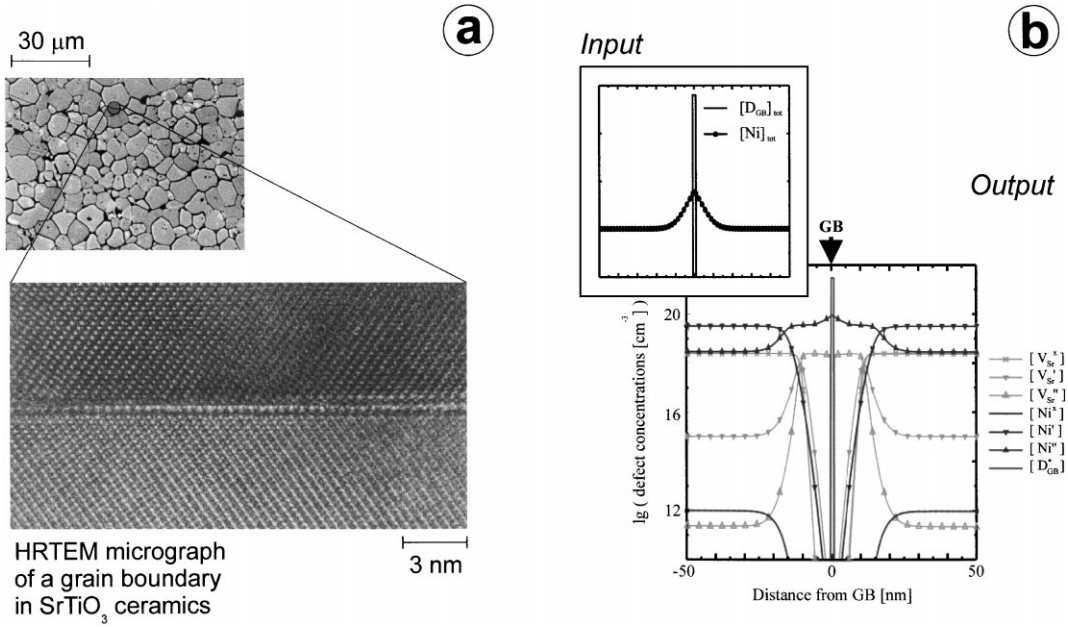

Fig. 13. Ceramic grain boundaries on the nanoscale: (a) micrograph of acceptor-doped $SrTiO_3$ ceramics, (b) input and output of a simulation of the defect chemistry and the electrostatics across the grain boundary.[39]

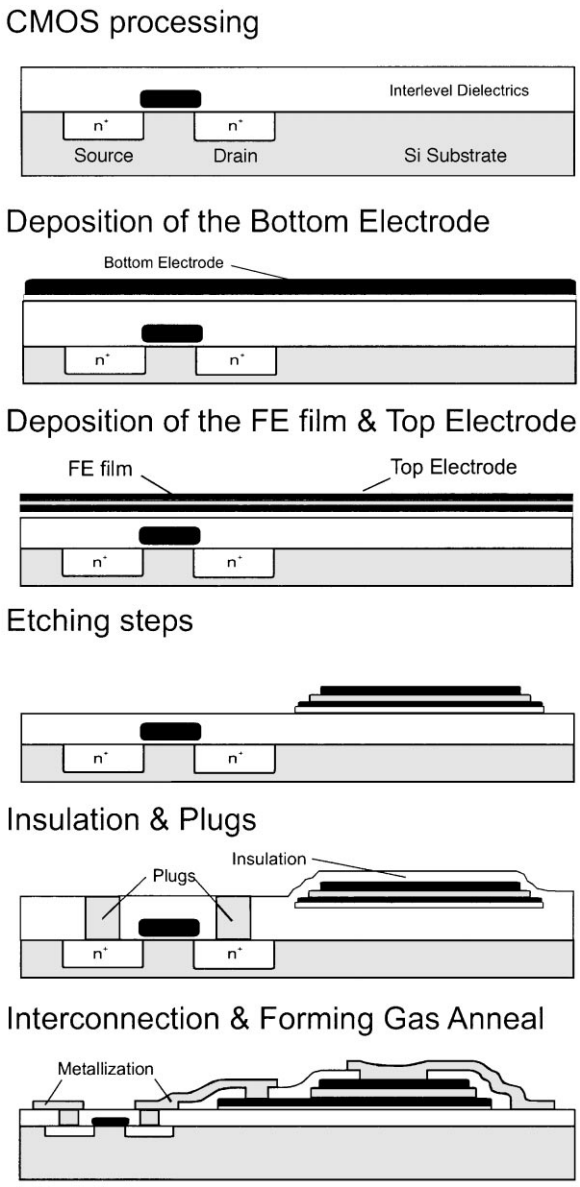

Fig. 14. Process sequence for the integration of electroceramic materials into the Si-based microelectronics.

4 Process Simulation

The third simulation layer treats all aspects of the technological realization of the devices. Figure 14 outlines the major processing steps for a low-density integration of an electroceramic capacitor on a Si-CMOS chip. All semiconductor integration steps are performed in a standard Si technology clean-room line (front-end line). This part is terminated by an ILD layer. All further steps are carried out in a back-end line. The chips do not re-enter the front-end line in order to avoid contamination of this line. After deposition of the bottom electrode, the dielectric or FE layer and the top electrode, appropriate etching steps are performed before the underlying Si structure is recessed, plugs are realized, and the metal interconnects and further isolation layers are applied. Finally, a forming gas anneal is used to improve the electronic properties of the SiO_2/Si interface of FETs and to increase the conductivity of poly-Si plug interfaces.

Critical issues of the integration of electroceramic films are: (1) the thermal budget, which may be narrow due to the relatively high crystallization temperatures of the ceramics, (2) the dry etching process due to the low volatility of the reaction products, (3) the forming gas annealing, which may deteriorate the properties of FE or dielectric capacitors, and (4) all cross-contamination problems.

5 Summary

For the integration of new, electroceramics-based functionalities into the standard Si microelectronics and microstructure technology world, new modeling approaches and extended simulation tools are required. This applies to all three levels of modeling, (1) circuit simulation, (2) device simulation, and (3) process simulation. The complexity of, e.g., the ferroelectric properties of appropriate oxides in conjunction with their microstructure and their electronic structure imposes a challenge on physically based modeling which by far exceeds the capabilities of present tools. Joint efforts in research and development are required to build up all relevant models at sufficient speed and to support the integration of new materials into industrial semiconductor technology.

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